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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/790,880	03/03/2004	Satoru Akiyama	500.43581X00	4729

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EXAMINER	
TRAN, DENISE	
ART UNIT	PAPER NUMBER
2185	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/26/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/790,880	AKIYAMA ET AL.	
	Examiner	Art Unit	
	Denise Tran	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 December 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) *13-17* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,6,10-12,18 and 19* is/are rejected.

7)☒ Claim(s) *4,5 and 7-9* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 10/790,880.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Applicant's election without traverse of Group I claims 1-12 and 18-19 in the reply filed on 12/21/06 is acknowledged.

2. Claims 13-17 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on 12/21/06.

3. Claims 1-12 and 18-19 are presented for examination.

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claim 18 is rejected under 35 U.S.C. 102(e) as being anticipated by Ooishi, US 2004/0027857.

Claim 18, Ooishi teaches a semiconductor device comprising:

a plurality of memory banks, each having plurality of memory cells (e.g., [0085] [0101]); and

a cache memory for communicating a write data to said plurality of memory banks (e.g., [0220]), wherein said memory cells include either SESO (Single Electron Shut Off) memory cells or phase change memory cells (e.g., [0280]), and said cache memory has a degree of association equal to or larger than a value (i.e., 0 or 1; e.g., [0220])) determined by a ratio (m/n) of a write cycle (m) of said memory cells to a read cycle (n) of said memory cells (i.e., 0 or 1; e.g., [0220])) determined by a ratio (m/n) of a write cycle (m) of said memory cells to a read cycle (n) of said memory cells (e.g., fig. 13, [0195]-[0202], a read cycle n and write cycle m at any clock cycle from 1 to 7, 0/2, 1/3).

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1, 3, 6, 10-12 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ooishi, US 2004/0027857, in view of Taylor et al., US 6,263,398 (hereinafter Taylor).

Claim 1, Ooishi teaches a semiconductor device comprising:

a plurality of memory banks, each having a plurality of memory cells which are slower in a write operation than in a read operation (e.g., [0085] [0101]); and

a cache memory for an access to said plurality of memory banks (e.g., [0220]), said cache memory having a number of way equal to or larger than a value (i.e., 0 or 1;

e.g., [0220])) determined by a ratio (m/n) of a write cycle (m) of said memory cells to a read cycle (n) of said memory cells (e.g., fig. 13, [0195]-[0202], a read cycle n and write cycle m at any clock cycle from 1 to 7, 0/2, 1/3). Ooishi does not explicitly show mediating an access to the memory from the outside. Taylor teaches a cache mediating an access to a memory from the outside (e.g., col. 3, lines 50 -60). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of Taylor into the system of Ooishi because it would allow faster access time.

Claims 3, 6, 10-12, and 19, Ooishi teaches a plurality of data input/output nodes for inputting/outputting data to/from the outside, wherein each said data input/output node has a data width equal to a data width of an external data bus for inputting/outputting information to/from said semiconductor device (e.g., data from input/output nodes to/from either BNKA, BNKB from/to an external bus; [[0092],[0101]); wherein each said memory cell is either a SESO (Single Electron Shut Off) memory cell or an phase change memory cell (e.g., [0280]), but does not explicitly show when said cache memory holds data corresponding to an access to said semiconductor device from the outside, the data is communicated from said cache memory; wherein said cache memory comprises SRAM memory cells. Taylor teaches when said cache memory holds data corresponding to an access to said semiconductor device from the outside, the data is communicated from said cache memory (e.g., col. 3, lines 50 –60; col. 9, line 20 and et seq.); wherein said cache memory comprises SRAM memory cells (e.g., abstract). It would have been obvious to one of ordinary skill in the art at the time

the invention was made to apply the teaching of Taylor into the system of Ooishi because it would allow faster access time.

7. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ooishi, US 2004/0027857, in view of Taylor et al., US 6,263,398 (hereinafter Taylor) as applied to claim 1 above, and further in view of Kook et al., US 20040015646 (hereinafter Kook).

Claim 2, the combination of Ooishi and Taylor does not explicitly show said cache memory has a plurality of sets corresponding to the number of ways, and each of said plurality of sets has a capacity for storing whole data stored in one of said plurality of memory banks. Kook shows a cache memory has a plurality of sets corresponding to the number of ways, and each of said plurality of sets has a capacity for storing whole data stored in one of a plurality of memory banks (e.g., fig. 2, cache 600, [0027]); It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of Kook into the system of Ooishi and Taylor because it would allow high speed data input/output and increase system performance.

8. Claims 4-5 and 7-9 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a) Hewitt et al. (5488711) shows a cache for mediating an access to an EEPROM device;

b) Garner (6704835) shows a multiple sets cache for mediating an access to a flash memory.

c) Bordui (US20040193782) shows a multiple cache banks.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Denise Tran whose telephone number is (571) 272-4189. The examiner can normally be reached on Monday and Thursday from 8:45 a.m. to 5:15 p.m.. The examiner can also be reached on alternate Friday

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sanjiv Shah, can be reached on 571-272-4098. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Denise Tran

2/16/07